

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application)	<u>PATENT APPLICATION</u>
Inventor(s): Wingyu Leung, et al.)	
Application No.: 10/645,861-7697)	Art Unit: 2133
Filed: 8/20/2003)	Examiner: Stephen M. Baker
Title TRANSPARENT ERROR CORRECTING MEMORY)	
)	

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.97

Mail Stop Amendment
 Commissioner for Patents
 P.O. Box 1450
 Alexandria, VA 22313-1450

Sir:

Listed below or on an attached Form PTO-1449 is information known to applicant(s). A copy of each listed publication and non-U.S. patent, is being submitted herewith, along with a concise explanation of information in a foreign language, if any, pursuant to 37 C.F.R. §1.97-1.98.

Applicants respectfully request that the listed information be considered by the Examiner and be made of record in the above-identified application. If form PTO-1449 is enclosed, the Examiner is requested to initial and return it in accordance with MPEP § 609.

This statement is not intended to represent that a search has been made or that the information cited in the statement is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56.

- This statement qualifies under 37 C.F.R. § 1.97, subsection (b) because (check all that apply):
- (1) It is being filed within 3 months of the application filing date and is other than a continued prosecution application under § 1.53(d)
-- OR --
 - (2) It is being filed within 3 months of entry of a national stage
-- OR --
 - (3) It is being filed before the mail date of the first Office Action on the merits.
-- OR --
 - (4) It is being filed before the mailing of a first Office Action after the filing of a request for continued examination under § 1.114

- 37 C.F.R. § 1.97(c). If this statement is being filed after the period specified in § 1.97(b), but before the mailing date of the earlier of a final office action under § 1.113, a notice of allowance under § 1.311, or an action that otherwise closes prosecution in the application, then:
- a certification as specified in § 1.97(e) is provided below; or
- a fee of \$180.00 as set forth in § 1.17(p) is authorized below, enclosed, or included with the payment of other papers filed together with this statement.
- 37 C.F.R. § 1.97(d). If this statement is being filed after the period specified in § 1.97(c), but on or before payment of the issue fee, then:
- A. a certification as specified in § 1.97(e) is completed below; and
- B. a fee of \$180.00 as set forth in § 1.17(p) is authorized below, enclosed, or included with the payment of other papers filed together with this statement.
- Fee Authorization.* The Commissioner is hereby authorized to charge the above-referenced fees of \$180 and charge any additional fees or credit any overpayment associated with this communication to Deposit Account No. 50-0574 (Docket No. MST-012-1P).

Respectfully submitted,

BEVER, HOFFMAN & HARMS, LLP

By: _____


E. Eric Hoffman, Reg. No. 38,186

Dated: November 8, 2006

Telephone: (925) 895-3545
Customer No. 22888

<p>Substitute for form 1449A/PTO</p> <p>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</p> <p>(Use as many sheets as necessary)</p>				Application Number	10/645,861-7697
				Filing Date	8/20/2003
				First Named Inventor:	Wingyu Leung
				Examiner: Stephen M. Baker	GROUP: 2133
Sheet	1	of	5	Attorney Docket Number	MST-012-1P

U.S. PATENT DOCUMENTS

Examiner Initials*	Cited No. ¹	Document Number Number - Kind Code ^{2/known}	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	F01	US-3,814,921	06/04/1974	Nibby et al.	
	F02	US-3,969,706	07/13/1976	Proebsting et al.	
	F03	US-4,045,783	08/30/1977	Harland	
	F04	US-4,389,714	06/21/1983	Nakao	
	F05	US-4,768,197	08/30/1988	Petolino et al.	
	F06	US-4,839,868	06/13/1989	Sato et al.	
	F07	US-4,884,271	11/28/1989	Concha et al.	
	F08	US-4,933,904	06/12/1990	Stewart et al.	
	F09	US-5,008,886	04/16/1991	Chinnaswamy et al.	
	F10	US-5,235,693	08/10/1993	Chinnaswamy et al.	
	F11	US-5,241,503	08/31/1993	Cheng	

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	F12	US-5,289,584	02/22/1994	Thome et al.	
	F13	US-5,369,651	11/29/1994	Marisetty	
	F14	US-5,402,389	03/28/1995	Flannagan et al.	
	F15	US-5,430,742	07/04/1995	Jeddeloh et al.	
	F16	US-5,469,558	11/21/1995	Lieberman et al.	
	F17	US-5,502,835	03/26/1996	Le et al.	
	F18	US-5,513,148	04/30/1996	Zagar	
	F19	US-5,519,839	05/21/1996	Culley et al.	
	F20	US-5,519,847	05/21/1996	Fandrich et al.	
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	F22	US-5,586,282	12/17/1996	Iimo et al.	

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	F23	US-5,592,435	01/07/1997	Mills et al.	
	F24	US-5,615,169	03/25/1997	Leung	
	F25	US-5,671,187	09/23/1997	Childers et al.	
	F26	US-5,687,353	11/11/1997	Chen et al.	
	F27	US-5,708,624	01/13/1998	Leung	
	F28	US-5,778,237	07/07/1998	Yamamoto et al.	
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	F30	US-6,020,773	02/01/2000	Kan et al.	
	F31	US-6,052,011	04/18/2000	Dasgupta	
	F32	US-6,701,480	B1	Karpluska et al.	
	F33	US-6,738,883	B2	March et al.	

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	F34	US-6,854,059	B2	02/08/2005	Gardner
	F35	US-7,064,993	B2	06/20/2006	Gyohten et al.
	F36	US-7,099,216	B2	08/29/2006	Luk et al.
	F37	US-2002/0029365	A1	03/07/2002	Sato et al.
	F38	US-2004/0039883	A1	02/26/2004	LaBerge et al.
	F39	US-2004/0044943	A1	03/04/2004	Jacquet et al.
	F40	US-2004/0064646	A1	04/01/2004	Emerson et al.
	F41	US-2004/0172504	A1	09/02/2004	Balazich et al.
	F42	US-2004/0213064	A1	10/28/2004	Gyohten et al.
	F43	US-2005/0185492	A1	08/25/2005	Harrand
	F44	US-2006/0034132	A1	02/16/2006	Jain

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	F45	US-2006/0080589	A1	04/13/2006	Holm et al.
	F46	US-2006/0156196	A1	07/13/2006	Takahashi et al.
	F47	US-2006/0158950	A1	07/20/2006	Klein
	F48	US-2006/0200723	A1	09/07/2006	Carnevale et al.
	F49	US-2006/0200728	A1	09/07/2006	Nagai et al.

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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	Bondurant, D. "15nsec Enhanced DRAM Upgrades System Performance in 72-Pin SIMM Socket", Silicon Valley Personal Computer Design Conference Proceedings, Date Unknown, pp. 81-86
	Dosaka et al. "A 100-Mhz 4-Mb Cache DRAM with Fast Copy-Back Scheme", IEEE Journal of Solid-State Circuits, Vol. 27, No. 11, Nov. 1992, pp. 1534-1539
	Sunaga et al. "A Full Bit Prefetch Architecture for Synchronous DRAM's", IEEE Journal of Solid-State Circuits, Vol. 30, No. 9, Sep. 1995, pp. 998-1005
	Pentium Processor 3.3V Pipelined BSRAM Specification, Ver. 2.0, Intel Corp., 25 May 1995, pp. 1-44

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